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Comparative Analysis of ASIC-Based and Conventional Control Techniques for SRM Drive Systems

Ms. Shaila P. Kharde¹, Dr. Ulhas D. Shiurkar²

Research Scholar, Dr.BAMU, Aurangabad (MS), India¹

Guide, DIEMS, Aurangabad (MS), India²

ABSTRACT: Switched Reluctance Motor (SRM) drives are widely used due to their robustness and suitability for electric vehicle. The performance of SRM drives depends heavily on the control technique used. This paper presents a comparative analysis of ASIC-based and conventional control methods, such as microcontroller and FPGA-based implementations. Key parameters including power consumption, processing speed, and real-time performance are evaluated. The ASIC-based approach demonstrates improved efficiency, faster operation, and lower power consumption, making it suitable for high-performance applications. In contrast, conventional methods offer greater flexibility and lower development cost. The study highlights the trade-offs between performance and adaptability, providing guidance for selecting appropriate control strategies for SRM drive systems.

KEYWORDS: Switched Reluctance Motor (SRM), ASIC, Control Techniques, Electric Vehicles (EVs), Comparative Analysis.

I. INTRODUCTION

Switched Reluctance Motor (SRM) drives have emerged as a promising solution for modern applications such as electric vehicles, industrial automation, and aerospace systems due to their simple construction, high reliability, and ability to operate under harsh conditions [9]. Unlike conventional motors, SRMs do not require permanent magnets or rotor windings, making them cost-effective and robust. However, their highly nonlinear characteristics and inherent torque ripple present significant challenges in achieving smooth and efficient operation, which makes the design of an effective control system essential [6].

Traditionally, SRM drive control has been implemented using microcontrollers and digital signal processors (DSPs), which offer flexibility and ease of programming [4], [10]. These platforms are widely used due to their simplicity and lower development cost. However, their sequential processing nature limits real-time performance, especially in high-speed applications.

More recently, Field Programmable Gate Arrays (FPGAs) have gained attention due to their parallel processing capability and improved real-time performance. FPGA-based SRM control systems provide faster execution, deterministic timing, and reduced latency compared to conventional controllers [1], [8]. They are also effective in implementing advanced control techniques such as torque ripple minimization and real-time simulation [3], [6]. Despite these advantages, FPGA-based designs involve higher complexity and require hardware-level expertise.

To overcome these limitations, Application-Specific Integrated Circuits (ASICs) are being explored as an advanced solution for SRM drive control. ASIC-based implementations enable optimized hardware design tailored for specific applications, resulting in higher operating speeds, lower power consumption, and improved system efficiency. However, ASICs lack flexibility and involve higher initial design complexity and cost.

This work focuses on a comparative analysis of ASIC-based and conventional control techniques for SRM drive systems. The study evaluates key performance parameters such as speed, power efficiency, latency, and hardware utilization, highlighting the trade-offs between performance optimization and design flexibility.

II. LITERATURE SURVEY

Switched Reluctance Motor (SRM) drives have gained significant attention due to their simple structure, robustness, and suitability for high-speed and electric vehicle applications. However, their performance is highly dependent on the control strategy and hardware implementation platform. Various technologies such as microcontrollers, DSPs, and FPGAs have been explored to enhance SRM drive performance.

2.1 Microcontroller/DSP-Based SRM Control

Microcontroller and DSP-based controllers are widely used for SRM drives due to their flexibility, low cost, and ease of implementation. These systems execute control algorithms sequentially, making them suitable for low and medium-performance applications [4], [10]. Advanced control techniques such as fuzzy logic and neuro-fuzzy controllers have been implemented on DSP platforms to handle nonlinear SRM characteristics and improve performance [10].

However, as system complexity increases, sequential execution leads to higher latency and reduced real-time performance. At high speeds, the controller struggles to process switching signals efficiently, limiting accuracy and efficiency [13], [19].

2.2 FPGA-Based SRM Control

To overcome the limitations of conventional controllers, FPGA-based implementations have gained significant attention. FPGAs support parallel processing, enabling faster execution and deterministic timing [1], [2].

Studies show that FPGA-based SRM controllers achieve high-speed operation with minimal delay and improved efficiency [1]. They are particularly effective for implementing complex control strategies such as torque ripple minimization and optimized switching angle control [6], [8]. FPGA-based observer designs also enhance performance across various speed ranges [7].

Additionally, FPGA platforms are widely used for real-time simulation and hardware-in-the-loop (HIL) testing, improving system validation and performance optimization [5].

Despite these advantages, FPGA-based systems require hardware design expertise and involve higher development complexity and cost.

2.3 Advanced Control Techniques

Recent research focuses on improving SRM performance using advanced control strategies. Techniques such as PWM control, current shaping, and torque-sharing functions are widely used to reduce torque ripple and improve efficiency [13], [19].

Sensorless control and rotor position estimation techniques are also important for reducing system cost and improving reliability [3]. Optimization of switching angles plays a key role in enhancing torque production and efficiency [8].

1. Hardware and Converter Considerations

The performance of SRM drives is also influenced by power converter topology and hardware design. Different converter configurations offer trade-offs between efficiency, cost, and complexity [15].

Accurate control of switching angles and fast sampling rates are critical for high-speed operation, which is better supported by FPGA-based systems compared to microcontrollers [1].

Most studies focus on either microcontroller/DSP or FPGA-based implementations, but comprehensive comparative analysis across multiple platforms is limited [3], [5]. FPGA-based systems provide high performance, but power optimization and hardware efficiency are not fully explored.

Limited research is available on ASIC-based SRM control in comparison with FPGA and microcontroller technologies. There is a need for integrated evaluation of speed, power consumption, latency, and cost trade-offs.

2. ASIC Drive for SRM

Cadence is the versatile tool for implementation of ASIC flow. For completing the ASIC flow, Cadence nlaunch tool is used for simulation of the described architecture, Cadence Genus RTL Compiler is used for synthesis and Cadence Innovus RTL to GDS software tool is used for converting the netlist into gdsII file format for fabrication. Adopting the ASIC design flow, the architecture is described using Very High-Speed Integrated Circuit Hardware Description Language (VHDL). The design is simulated by invoking nlaunch and running in Multiple Step Execution mode. Beginning with nlaunch mode selection and parameter definition, simulation is executed in three steps: Compilation, Elaboration and Simulation

While Physical designing, the verilog netlist file is imported and parameters are set to the design requirements. With the initial unplanned area, Floorplanning parameters like Core Size and Die Size are assigned. In the design, General Purpose Design Kit (GPDK) library files are used for implementation by using slow and fast library for worst case and best-case path analysis. Analysis is done for crucial parameters like Power, Area, Gate Count and Time.

Table 1 Comparison of ASIC and different FPGA

Sr. No.	FPGA Device	Total Power (W)	Timing Period (ns)	Frequency (MHz)	Resource Utilization (Total Complexity)
1	Stratix V (5SGXEA7N2F45C2) (High Performance)	0.326	3.727	268.46	200
2	Arria 10 (10AX048H2F34E2SG) (Low Power)	0.184	3.196	312.89	200
3	Stratix 10 (1SG280HU2F50E2VG) (Ultra Performance)	0.517	2.372	421.77	200
4	Cyclone V (5CSEMA5F31C6) (Embedded / Industrial)	0.097	6.740	148.40	198
5	Cyclone IV E (EP4CE115F29C7) (Cost Optimized)	0.077	7.892	126.78	200
6	Cyclone 10 GX (10CX150YF780I5G) (Automotive / Industrial)	0.113	5.446	183.55	200
7	Arria V (5AGXFB3H4F35C4) (Defense / Industrial)	0.214	4.507	221.90	200
8	Stratix IV (EP4SGX530KF40C2) (Defense Grade)	0.265	4.171	239.67	200
9	Cadence 180nm	0.17595454	1.704248	586.769062	535
10	Cadence 90nm	0.1078	1.13674	879.70864	507
11	Cadence 45nm	0.01113636	0.749014	1335.08853	323

III. CONCLUSION

The prime objective of the proposed research work is to design and develop an application specific integrated circuit for switched reluctance motor drive for targeting to the transport vehicle. The architecture of the proposed system is described using Very High-Speed Integrated Circuit Hardware Description Language (VHDL). For execution of the different steps in the FPGA design flow, Altera Quartus High Level Synthesis (HLS) tool is used.

This tight optimization cannot be done using FPGA design flow, because FPGA is the pre-compiled architecture of the different hardware components.

The solution is with the Application Specific Integrated Circuit (ASIC) design flow. In ASIC flow, only required components are fabricated in the integrated circuit hence tight optimization is observed with respect to the time, frequency, resource utilization and power utilization.

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